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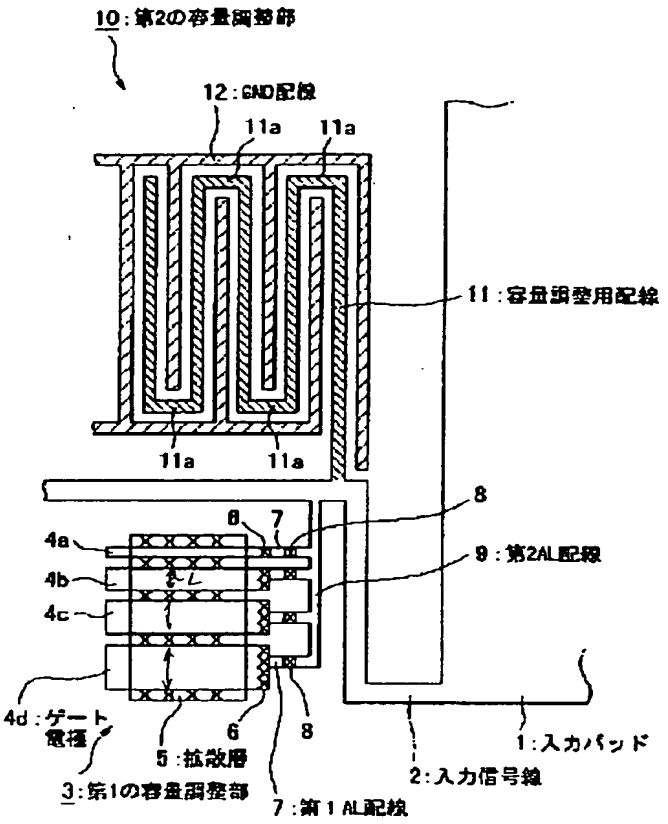
TITLE : SEMICONDUCTOR DEVICE



ABSTRACT : PROBLEM TO BE SOLVED: To provide a semiconductor device equipped with a capacitance adjusting part for freely setting the adjusting amounts of a wiring capacitance, and for easily operating the adjusting work.

SOLUTION: A semiconductor device is provided with a conventional capacitance adjusting part 3 and a capacitance adjusting part 10, in which a prescribed wiring capacitance is formed by adjacently arranging capacitance adjusting wiring 11 constituted of second aluminum wiring connected with an input signal line 2 for adjusting the wiring capacitance, and GND wiring 12 constituted of the second aluminum wiring in the same layer as the capacitance adjusting wiring 11 for adjusting the wiring capacitance of the input signal line 2 based on the wiring capacitance.

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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by providing the following. Wiring for capacity adjustment connected to the capacity-ed adjustment wiring which is going to adjust wiring capacity. The capacity controller the constant-voltage wiring with which fixed voltage was impressed is formed while being formed in the same layer as this wiring for capacity adjustment, contiguity arrangement of the aforementioned wiring for capacity adjustment and the aforementioned constant-voltage wiring is carried out, and predetermined line capacity is formed, and adjust the wiring capacity of the aforementioned capacity-ed adjustment wiring by this line capacity.
[Claim 2] The semiconductor device according to claim 1 with which the aforementioned constant-voltage wiring is characterized by being supply voltage wiring or grounding voltage wiring.
[Claim 3] The semiconductor device according to claim 1 or 2 characterized by the thing of the aforementioned wiring for capacity adjustment, and the aforementioned constant-voltage wiring for which either has a flection at least.
[Claim 4] The semiconductor device according to claim 1 or 2 characterized by the thing of the aforementioned wiring for capacity adjustment, and the aforementioned constant-voltage wiring for which either was formed in the shape of a ctenidium at least.
[Claim 5] The semiconductor device according to claim 1 to 4 with which the aforementioned capacity controller is characterized by the bird clapper from the wiring formed in the best layer of the multilayer-interconnection structures.
[Claim 6] The semiconductor device according to claim 5 characterized by preparing the aforementioned capacity controller above the arbitrary elements which consisted of layers except the aforementioned best layer, or wiring in piles.
[Claim 7] The semiconductor device according to claim 1 to 6 with which the aforementioned capacity-ed adjustment wiring is characterized by being an input signal line.
[Claim 8] The semiconductor device according to claim 1 to 6 with which the aforementioned capacity-ed adjustment wiring is characterized by being a clock signal line in a circuit.
[Claim 9] The semiconductor device characterized by having the capacity controller which the input pad which consists of a two-layer conductive layer arranged through an insulating layer is prepared, and the capacity between layers is formed of a conductive layer two-layer [these], and adjusts the wiring capacity of input signal wiring with this capacity between layers.
[Claim 10] The semiconductor device according to claim 9 characterized by adjusting the aforementioned capacity between layers by whether for one [which constitutes this capacity controller / at least] conductive layer to be divided into two or more fields,

and to short-circuit the aforementioned two-layer conductive layer for every division field of these plurality in the aforementioned capacity controller.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the semiconductor device equipped with the capacity controller for adjusting wiring capacity easily and rationally about a semiconductor device.
[0002]
[Description of the Prior Art] Drawing 6 shows an example of the composition of the conventional DRAM. From the former, by semiconductor devices, such as DRAM, the miniaturization of a package has been energetically advanced so that packaging density may not fall, even if chip area increases by increase of storage capacity. What is shown in drawing 6 is CSP (Chip Size Package) which is one of the packages to which the miniaturization progressed most adopted in recent years. It is an example. The substrate 100 and semiconductor chip 101 which consist of a polyimide turn a chip front-face side to a substrate side, and are fixed, and this CSP is closed with a resin 102. While many solder balls 103 used as an external terminal are formed in the inferior surface of tongue of a substrate 100, many pads (illustration abbreviation) used as the wiring terminal on a chip are formed in the front face of a semiconductor chip 101. And each solder ball 103 and each pad are electrically connected through the conductor (illustration abbreviation) embedded in the copper wiring (illustration abbreviation) formed in the substrate upper surface, and the through hole which penetrates a substrate.
[0003] Drawing 7 is the outline block diagram showing the circuit block of a semiconductor chip. This chip has four memory cell blocks 104 and the circumference circuit 105 arranged at the circumference, and many pads 106 are formed in the center of a chip at one train. In addition, in this drawing, illustration of the wiring which leads to a pad 106 is omitted.
[0004] Drawing 8 shows the state where Above DRAM was seen from the rear-face side (solder ball side). In the example of this DRAM, three trains of solder balls 103 on a substrate 100 are arranged at each right and left, and the pad 106 on a semiconductor chip 101 is arranged in the center at one train. Therefore, the wiring 107 which connects each pad 106 with each solder ball 103 cannot wire linearly, though natural, but it is managed suitably and it is wired so that it may not connect with other wiring 107 too hastily. In addition, although only a part of wiring 107 which connects a pad 106 with the solder ball 103 was illustrated in drawing 8 , other parts are wired similarly.

[0005] However, since length differs every wiring 107 so that clearly even if it sees drawing 8 , the wiring capacity which each wiring 107 has also differs for every wiring. That is, the wiring capacity from the external terminal of DRAM to a pad will vary between pins, with this, on the occasion of the writing of data, and read-out operation, the timing of a signal shifts between pins, and there is a possibility of leading to generating of an error. Then, in this kind of semiconductor chip, the capacity controller for performing a double lump of the wiring capacity of each wiring is usually prepared.
[0006] Drawing 9 is drawing showing the composition of the capacity controller of Above DRAM. This capacity controller 108 consists of gate capacitances fundamentally. That is, capacity is formed through the diffusion layer 109 formed in the semiconductor substrate front face, and the gate insulator layer of a diffusion layer 109 and the gate electrodes 110a, 110b, 110c, and 110d which counter. moreover, in order to boil and adjust various capacity value, the gate electrodes 110a, 110b, 110c, and 110d of plurality (four pieces in this case) are formed, and each gate electrodes 110a, 110b, 110c, and 110d connect with the 1st aluminum wiring 112 through a through hole 111, respectively -- having -- every -- the 1st aluminum wiring 112 is connected to the 2nd aluminum wiring 114 through the through hole 113, respectively And each 2nd aluminum wiring 114 is connected to the input signal line 116 connected to the input pad 115.
[0007] In addition, in this specification, the near (lower layer side) 1st layer [in / two-layer wiring structure / in "the 1st aluminum wiring"] wiring / aluminum / and the "2nd aluminum wiring" mean the aluminum wiring by the side of a two-layer eye (upper layer side).
[0008] Gate lengths differ, respectively and, as for the four above-mentioned gate electrodes 110a, 110b, 110c, and 110d, each is set as double precision, 3 times, and 4 times as many gate length as this on the basis of the minimum gate length. If it is based on the capacity value of the place of the minimum gate length also about capacity value according to it, it is double precision, 3 times, and 4 times as many capacity value as this. That is, capacity value is set up in order towards the greatest gate length like 10fF(s) (FEMUTO farad), 20fF, 30fF, and 40fF from the minimum gate length.
[0009] In DRAM equipped with such a capacity controller 108, when a double lump of wiring capacity is performed, after assembling the semiconductor chip in the state of a package and performing measurement of an electrical property, and evaluation, addition of capacity was adding capacity using the above-mentioned capacity controller 108 to the required input signal line so that it might double with a side with much wiring capacity judging from this evaluation result. When capacity was actually added, the design change of the mask pattern of the 2nd aluminum wiring was carried out, and the capacity value to add was changed by any of a gate capacitance with the four above-mentioned kinds of capacity value are connected to an input signal line. Therefore, in the case of the above-mentioned example, it comes out [the capacity addition from 10fF to 100fF(s) 10-fF(s)-cuts fine with the combination of four kinds of gate capacitances, and] and was possible.
[0010]
[Problem(s) to be Solved by the Invention] However, there were the following troubles in the adjustment method of the wiring capacity in the above-mentioned conventional DRAM. That is, in order that capacity value might adjust wiring capacity combining some kinds of gate capacitances fixed respectively, only adjustment by the limited serration width of face (they will be 10fF(s) if it says in the above-mentioned example), or the limited upper limit (they will be 100fF(s) if it says in the above-mentioned example) could be performed, but adjustment of fine capacity value was difficult. Although it is possible to prepare many gate capacitances including the thing

of smaller capacity value as the cure, the occupancy area of a capacity controller will increase because the number of gate capacitances increases in that case, and the problem of leading to increase of chip area will arise. Moreover, when adding a new gate capacitance, a design change is needed from a lower layer mask pattern, and there is also a problem that the time and effort and time of a mask design change increase.
[0011] this invention is made in order to solve the above-mentioned technical problem, it can set up the amount of adjustments of wiring capacity free, and aims at offering the semiconductor device equipped with the capacity controller of the structure where the tuning can moreover be performed easily.
[0012]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the semiconductor device of this invention has the following two solution meanses. First, the wiring for capacity adjustment to which the 1st semiconductor device of this invention was connected to the capacity-ed adjustment wiring which is going to adjust wiring capacity, The constant-voltage wiring with which fixed voltage was impressed while being formed in the same layer as the wiring for capacity adjustment is formed. Contiguity arrangement of the wiring for capacity adjustment and the constant-voltage wiring is carried out, and predetermined line capacity is formed and it is characterized by having the capacity controller which adjusts the wiring capacity of capacity-ed adjustment wiring by this line capacity. For example, supply voltage wiring, grounding voltage wiring, etc. can be used for the aforementioned constant-voltage wiring. And as a configuration of the wiring for capacity adjustment, or constant-voltage wiring, it can have a flection or can form in the shape of a ctenidium.
[0013] That is, to the conventional capacity controller having used the gate capacitance, contiguity arrangement of the wiring for capacity adjustment and the constant-voltage wiring is carried out, and the capacity controller of the 1st semiconductor device of this invention forms line capacity with these wiring. And the wiring for these capacity adjustment and constant-voltage wiring can obtain capacity value predetermined in a limited occupancy area, if the opposed face product of wiring is enlarged by it not only merely arranging in the shape of a straight line, but making it crooked, or arranging so that wiring of two may be engaged as a ctenidium-like configuration. Moreover, the change in the opposed face product of wiring can adjust the size of capacity value to add free.
[0014] Consequently, according to this invention, a semiconductor device with the high reliability which the error which originated in the timing gap of the signal between pins on the occasion of the writing of data and read-out operation does not produce can be offered.
[0015] As for the aforementioned capacity controller, it is desirable to form with the wiring formed in the best layer of the multilayer-interconnection structures. When it considers as this composition, capacity value can be adjusted only by change of the mask pattern of the wiring layer of the best layer, and the mask pattern by the side of a lower layer does not need to add the hand of correction at all rather than it. Therefore, the time and effort and time of a mask design change concerning adjustment of wiring capacity can be reduced.
[0016] Furthermore, when a capacity controller is formed with wiring of the best layer, the capacity controller can be formed above the arbitrary elements which consisted of layers except the best layer, or wiring in piles. If it does in this way, since a space is not separately needed for a capacity controller, it can contribute to reduction-ization of chip area.
[0017] Here, as wiring used as the object which adjusts the aforementioned wiring capacity, and "capacity-ed adjustment wiring" said by this invention, an input signal

line or the clock signal line in a circuit can be considered.
[0018] Next, an input pad is constituted by the two-layer conductive layer arranged through an insulating layer, a conductive layer two-layer [these] forms the capacity between layers, and the 2nd semiconductor device of this invention is characterized by having the capacity controller which adjusts the wiring capacity of input signal wiring with the capacity between this layer. In this capacity controller, as one of the concrete methods which performs capacity adjustment, one [which constitutes a capacity controller / at least] conductive layer can be divided into two or more fields, and whether a two-layer conductive layer is short-circuited for two or more division fields of every can adjust the capacity between layers.
[0019] That is, the capacity controller of the 2nd semiconductor device of this invention forms the capacity between layers by the two-layer conductive layer which constitutes an input pad. Usually, since the area and layer insulation layer thickness of an input pad are the regular value, they become only a value also with the fixed value of the capacity between layers which consists of a conductive layer two-layer [these]. Then, the contact which divides into plurality the conductive layer which constitutes an input pad, for example, connects a two-layer conductive layer for two or more division fields of every is formed, and if a two-layer conductive layer is short-circuited and a two-layer conductive layer will not be short-circuited as the division field does not form capacity and contact is not formed conversely, the division field will form the capacity between layers. Therefore, if the number of the division fields which short-circuit a two-layer conductive layer is fluctuated, when it sees as the whole input pad, the value of the capacity between layers can be adjusted.
[0020] Since this means does not need a space new in order to use the input pad which occupies latus area to some extent originally as a capacity controller and to prepare a capacity controller, it is a very effective means from a viewpoint of reduction of the occupancy area of a capacity controller. Furthermore, there is an advantage that the large amount of capacity adjustments can also be taken. Moreover, capacity adjustment of fine serration width of face is also possible by dividing a conductive layer finely.
[0021] In addition, although the capacity controller which consists of the conventional gate capacitance may be altogether transposed to the above 1st and the capacity controller of the semiconductor device of the 2nd this invention as long as it can do, this invention is not limited to it and may use together suitably the conventional capacity controller, and the 1st of this invention and the 2nd capacity controller. For example, after giving the capacity of the grade which has used the conventional capacity controller, you may be made to tune wiring capacity finely using the capacity controller of this invention. By doing so, both capacity controllers can collaborate and it can contribute to adjustment of wiring capacity.
[0022]
[Embodiments of the Invention] The gestalt of operation of the 1st of this invention is explained with reference to a drawing below [the gestalt of the 1st operation].
Drawing 1 is drawing showing DRAM (semiconductor device) of the gestalt of this operation, and shows the composition of the capacity controller which is especially the feature portion of this invention. In addition, the wiring structure of DRAM of the gestalt of this operation consists of two-layer aluminum wiring.
[0023] In the gestalt of this operation, the wiring (capacity-ed adjustment wiring) used as the object which is going to adjust wiring capacity is the input signal line 2 connected to the input pad 1. And this input signal line 2 is formed with the 2nd aluminum wiring. As shown in drawing 1 , with the gestalt of this operation, the conventional capacity controller (henceforth the 1st capacity controller 3) is used for

capacity adjustment. That is, the 1st capacity controller 3 which consisted of gate capacitances is formed, each of four gate electrodes 4a, 4b, 4c, and 4d formed on the diffusion layer 5 is connected to the 1st aluminum wiring 7 through a through hole 6, each 1st aluminum wiring 7 is connected to the 2nd aluminum wiring 9 through a through hole 8, and the 2nd aluminum wiring 9 is connected to the input signal line 2. It is set as 10fF(s), 20fF, 30fF, and 40fF as an example, and the capacity addition from 10fF(s) to 100fF(s) 10-fF(s)-cuts fine with the combination of four kinds of gate capacitances, it comes out, and the capacity value of each gate capacitance is possible. Here, all gate capacitances are connected to the input signal line 2, and the capacity of a total of 100 fF(s) is added.

[0024] Furthermore, in addition to the 1st capacity controller 3, the capacity controller (henceforth the 2nd capacity controller 10) peculiar to this invention is used together to adjustment of wiring capacity with the form of this operation. If the composition of the 2nd capacity controller 10 is explained, it branches from the middle of the input signal line 2, and the wiring 11 for capacity adjustment which has four flection 11a is formed. It is formed with the 2nd aluminum wiring like [this wiring 11 for capacity adjustment] the input signal line 2. The ground wiring 12 (it is described as GND wiring constant-voltage wiring and the following) which branched from the main ground wiring (not shown) passing through the inside of a chip on the other hand is formed in the shape of a ctenidium so that it may gear with the configuration where the wiring 11 for capacity adjustment was crooked. It is formed with the 2nd aluminum wiring as well as [the GND wiring 12] the wiring 11 for capacity adjustment. And proximity arrangement is carried out so that the wiring 11 for capacity adjustment and the GND wiring 12 may counter mutually, and the line capacity of about several 100 fFs is formed. The 2nd capacity controller 10 which adjusts the wiring capacity of the input signal line 2 by this line capacity is constituted. In addition, in order to make a drawing legible in drawing 1 , hatching was performed to the wiring 11 for capacity adjustment, and the GND wiring 12.

[0025] In DRAM of the gestalt of the above 1st and this implementation equipped with the 2nd capacity controller 3 and 10, in performing a double lump of the wiring capacity of the input signal line between each pin What is necessary is just to add capacity using the 1st and 2nd capacity controller 3 and 10 so that it may double with a side with much wiring capacity judging from this evaluation result after assembling a semiconductor chip in the state of a package and performing measurement of an electrical property, and evaluation. That is, since DRAM of the gestalt of this operation is equipped with the 1st and 2nd capacity controller 3 and 10, in the case of adjustment of the wiring capacity of the input signal line 2, wiring capacity can be adjusted appropriately, making full use of the capacity controllers 3 and 10 of these both sides. For example, what is necessary is to add 100fF(s) which are the maximum capacity in the 1st capacity controller 3 to wiring capacity, and just to use the 2nd capacity controller 10, when capacity is still insufficient. The capacity value to add can be finely adjusted by adjusting suitably the length of the wiring 11 for capacity adjustment, and the GND wiring 12, and adjusting the opposed face product of these wiring 11 and 12 in that case.

[0026] Thus, in DRAM of the gestalt of this operation, desired wiring capacity can be realized with high degree of accuracy, without enlarging occupancy area of a capacity controller so much, since the 2nd capacity controller 10 consists of the wiring 11 for capacity adjustment and the ctenidium-like wiring [GND] 12 which were made crooked. Under the present circumstances, what it opts for is the 2nd aluminum wiring, and whether it has set to the 1st capacity controller 3, and the gate capacitance of a gap is connected to the input signal line 2 Since the 2nd aluminum wiring also

adjusts the length of the wiring 11 for capacity adjustment, and the GND wiring 12 in the 2nd capacity controller 10 Only the pattern of the 2nd aluminum wiring is sufficient for the mask pattern changed on the occasion of adjustment of wiring capacity, and the mask pattern by the side of a lower layer does not need to add the hand of correction at all rather than it. Therefore, the time and effort and time of a mask design change concerning adjustment of wiring capacity can be reduced.

[0027] In the gestalt of this operation, although the 2nd capacity controller 10 was constituted from the wiring 11 for capacity adjustment and the ctenidium-like wiring [GND] 12 which have four flection 11a, various design changes are possible for the concrete configuration of the wiring for capacity adjustment, and GND wiring, without restricting to this. For example, as shown in drawing 2 , it is good also as 2nd capacity controller 16 of a configuration which makes the both sides of the wiring 14 for capacity adjustment, and the GND wiring 15 the shape of a ctenidium, and engages ctenidiums. Even when it does in this way, it becomes possible like drawing 1 to adjust wiring capacity value free.

[0028] The gestalt of operation of the 2nd of this invention is explained with reference to a drawing below [the gestalt of the 2nd operation]. Drawing 3 is drawing showing DRAM (semiconductor device) of the gestalt of this operation, and shows the composition of the capacity controller which is especially the feature portion of this invention.

[0029] Although the gestalt of the 1st operation showed the example which used together the 1st capacity controller 3 of structure, and the 2nd capacity controller 10 peculiar to this invention conventionally in adjustment of the wiring capacity of the input signal line 2, with the gestalt of this operation, wiring capacity is adjusted only by the 2nd capacity controller 10, without using the 1st capacity controller 3. namely, the composition of the 2nd capacity controller 10 which consists of wiring 11 for capacity adjustment, and GND wiring 12 in drawing 3 -- the gestalt of the 1st operation -- being the same (the same sign being attached about drawing 1 and a common component) -- no four gate capacitances which constitute the 1st capacity controller 3 are connected to the input signal line 2

[0030] Thus, DRAM of the gestalt of this operation is an example which pays all the capacity added at the time of adjustment of wiring capacity by the 2nd capacity controller 10. Also in the gestalt of this operation, the same effect as the gestalt of the 1st operation that the time and effort and time of a mask design change concerning the adjustment of wiring capacity which can realize desired wiring capacity with high degree of accuracy can be reduced without enlarging occupancy area of a capacity controller can be done so.

[0031] Although the 1st capacity controller 3 and the 2nd capacity controller 10 were formed in the separate part in the gestalt of the 1st and the 2nd operation, the 1st capacity controller 3 is formed by the gate capacitance, and since the 2nd capacity controller 10 is formed only with the 2nd aluminum wiring, it can still also form the 2nd capacity controller 10 above the 1st capacity controller 3 in piles. Since the 1st capacity controller 3 is not used especially in the case of the gestalt of the 2nd operation, the 2nd aluminum wiring does not exist above the 1st capacity controller 3 at all, but the wiring 11 for capacity adjustment and the GND wiring 13 which make the 2nd capacity controller 10 can be arranged freely. Or as long as there is a part in which the 2nd aluminum wiring does not exist in other parts, you may form the 2nd capacity controller 10 there. By considering as such composition, much more reduction of the occupancy area of a capacity controller can be aimed at, and it can contribute to reduction-ization of chip area.

[0032] In addition, in the gestalt of the 1st and the 2nd operation, although the

example which constitutes the 2nd capacity controller 10 from wiring 11 for capacity adjustment and GND wiring 12 was shown, a capacity controller may consist of wiring for capacity adjustment, and supply voltage wiring (VDD wiring). Even in such a case, the same effect as the gestalt of the above-mentioned implementation can be acquired. Although it is easy to use GND wiring and VDD wiring as constant-voltage wiring used for the capacity controller of this invention, you may use it, as long as a suitable part has the wiring with which fixed voltage was always impressed in addition to these wiring.

[0033] The gestalt of operation of the 3rd of this invention is explained with reference to a drawing below [the gestalt of the 3rd operation]. Drawing 4 is drawing showing DRAM (semiconductor device) of the gestalt of this operation, and shows the composition of the capacity controller which is especially the feature portion of this invention. Moreover, drawing 5 is a cross section which meets the A-A line of drawing 4 . In addition, it is two-layer aluminum wiring structure as well as the wiring structure 1st of DRAM of the gestalt of this operation, and the gestalt of the 2nd operation.

[0034] The 1st aluminum layer 20 (conductive layer) and the 2nd aluminum layer 21 (conductive layer) which constitute the input pad 19 form the capacity between layers through the layer insulation film 22, and the capacity controller 18 of DRAM of the gestalt of this operation adjusts the wiring capacity of the input signal line 23 with the capacity between this layer, as shown in drawing 5 . As this capacity controller 18 is shown in drawing 4 and drawing 5 , the 1st aluminum layer 20 is divided into the fields 24a and 24b of plurality (a total of 16 of four-line four trains when it is the gestalt of this operation). In drawing 4 among these division fields 24a and 24b and to a total of nine division field 24a of eye eye one train from the left-hand side of the upper shell of the 2nd line, the 3rd line, and the 4th line, and 2 train, and eye three trains As shown in drawing 5 , two or more (in the case of the gestalt of this operation nine pieces) contacts 25 which the layer insulation film 22 is penetrated [contacts] and short-circuit the 1st aluminum layer 20 and the 2nd aluminum layer 21 are formed in each division field 24a of every. Moreover, in drawing 4 , contact 25 is not formed in a total of seven division field 24b of a top line and a rightmost train, and has not connected the 1st aluminum layer 20 and the 2nd aluminum layer 21 with it too hastily.

[0035] In the capacity controller 18 of the gestalt of this operation, the 1st aluminum layer 20 which constitutes the input pad 19 is divided into two or more fields 24a and 24b, and field 24a in which contact 25 was formed, and field 24b which is not formed are made. A part beam sake, In field 24a in which contact 25 was formed, the two-layer aluminum layers 20 and 21 short-circuit. The division field 24a does not form capacity, but in the field 24b in which contact 25 is not formed on the other hand, since the two-layer aluminum layers 20 and 21 do not short-circuit, the division field 24b will form capacity. Therefore, in the case of the gestalt of this operation, the capacity 7 times the capacity of between layers obtained by one division field 24b decided by the area of division field 24b and thickness of the layer insulation film 22 can be added to wiring capacity. Therefore, by fluctuating the number of division field 24b which does not short-circuit the two-layer aluminum layers 20 and 21, the value of the capacity between layers can be adjusted as the whole pad, and the amount of adjustments of wiring capacity can be changed.

[0036] Since the capacity controller 18 of the gestalt of this operation does not need a new space in case it tends to use the input pad 19 which occupies latus area to some extent as a capacity controller and prepares a capacity controller, it is an effective method from a viewpoint of reduction of the occupancy area of a capacity controller. Furthermore, there is an advantage that the area of input pad 19 the very thing can also take the large amount of capacity adjustments for a latus reason. Moreover, capacity

adjustment of fine serration width of face is also possible by dividing the 1st aluminum layer 20 more finely.

[0037] in addition, the technical range of this invention can add various change in the range which is not limited to the gestalt of the above-mentioned implementation and does not deviate from the meaning of this invention For example, although the gestalt of the 1st and the 2nd operation showed the case of an input signal line as wiring of the object which performs capacity adjustment, the candidate for application of the capacity controller of this invention may not be restricted to an input signal line, and may be a clock signal line in a circuit etc. Furthermore, when there is wiring which wants to make timing late intentionally not only the purpose of doubling the timing of a signal among two or more pins but in a circuit, you may use the capacity controller of this invention in order to add capacity to the wiring. Moreover, you may use together suitably the conventional capacity controller, the 1st, the capacity controller that consists of line capacity of the gestalt of the 2nd operation, and the capacity controller which consists of capacity between layers of the input pad section of the gestalt of the 3rd operation.

[0038] Of course about the number of flections, such as the concrete configuration of the capacity controller shown with the gestalt of the above-mentioned implementation, for example, the wiring for capacity adjustment, and GND wiring, the number of ctenidiums, the number of the division fields of the input pad section, etc., it can change suitably. Moreover, the scope of this invention cannot be restricted to DRAM of two-layer wiring structure, and can be applied to the various semiconductor devices which have multilayer-interconnection structure.

[0039]

[Effect of the Invention] As mentioned above, as explained in detail, in the semiconductor device of this invention, the wiring capacity of capacity-ed adjustment wiring can be adjusted free by fluctuating the opposed face product of the wiring for capacity adjustment, supply voltage wiring or the wiring for capacity adjustment, and grounding voltage wiring, or fluctuating the number of the division fields which do not short-circuit a two-layer conductive layer. Consequently, a semiconductor device with the high reliability which the error which originated in the timing gap of the signal between pins on the occasion of the writing of data and read-out operation does not produce can be offered. Moreover, the effect that the time and effort and time of a mask design change concerning wiring capacity adjustment can be reduced, or reduction-ization of chip area can be attained by reducing the occupancy area of a capacity controller can also be acquired.

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